IDEC Chip Design Contest

A 64-bit Prefix Adder based on Semidynamic and Bypassing Structures

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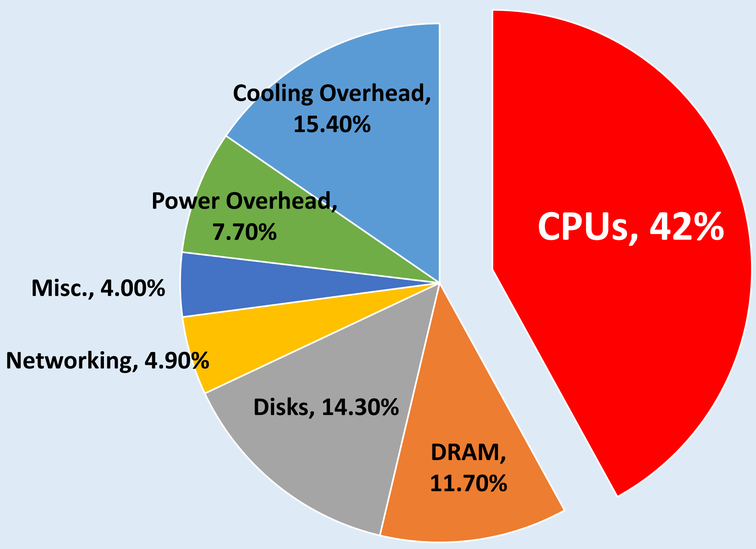
1. Motivation

Peak Power Breakdown in a Google Datacenter*

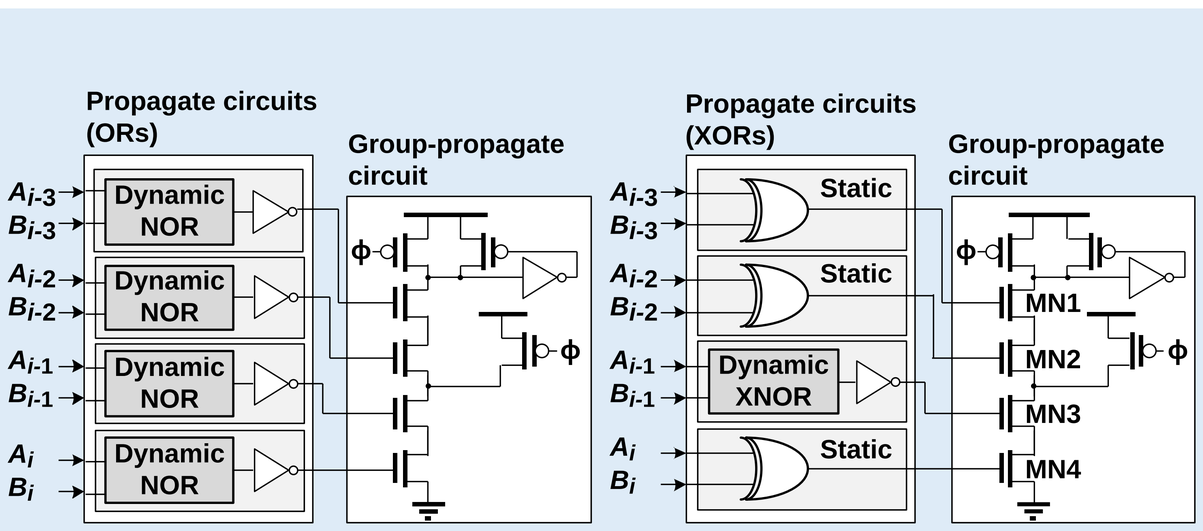


- ❑ Most power-hungry CPUs in server systems.
  - A large amount of heat dissipation occurs in CPUs
  - Cooling cost greatly depends on CPUs
- ❑ Adders in CPUs
  - Essential component for computation
  - Thermal hotspot in a CPU**

⇨ **High-speed and low-power adder is one of the most critical blocks in server processors**

* L. Barroso et al., *Second Edition, Morgan & Claypool Publishers*, 2013
**S.-S. Park et al., *electronics*, Jan. 2020

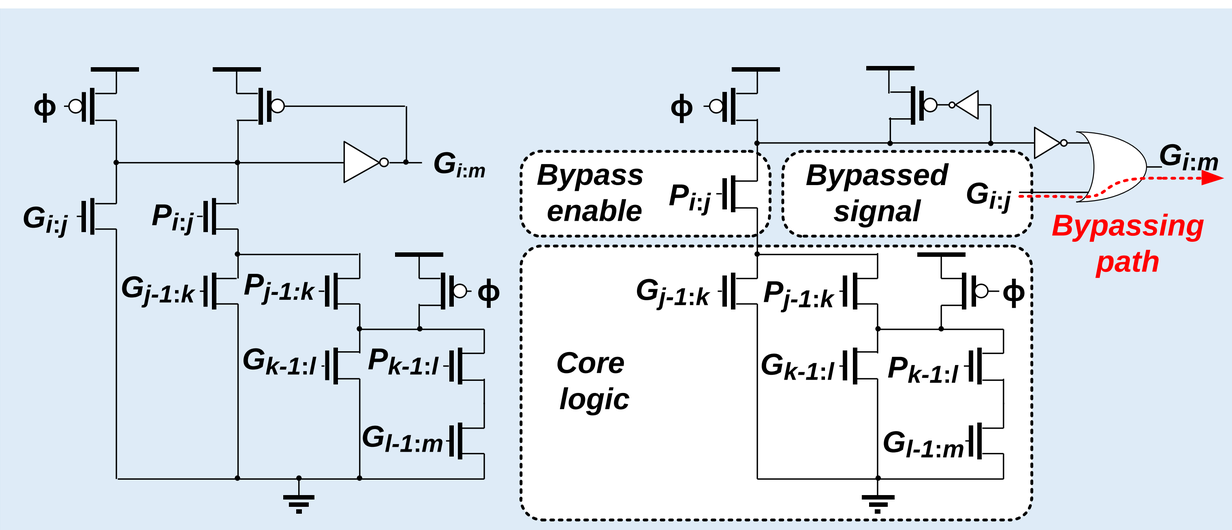
2. Architecture



Conventional Structure | **Proposed Semidynamic Structure**

- ❑ Semidynamic propagate circuit
  - Leverages both dynamic and static circuits for energy-efficiency

  ⇨ 17.9% power saving



Conventional Group-Generated Circuit | **Dynamic Bypassing Group-Generate Circuit**

- ❑ Dynamic bypassing group-generate circuit
  - Reduces switching probability of dynamic circuit by exploiting bypassing technique

  ⇨ Additional 5.2% power saving

3. Result

	Conventional semidynamic adder**	Semidynamic (proposed)	Semidynamic bypassing adder (proposed)
Technology	0.18 μm	0.18 μm	0.18 μm
Word length	64-bit	64-bit	64-bit
Power (mW)	134	110	103
Delay (ps)	480	505	505
PDP (pJ)	64.3	55.6	52.0

Note: Conventional adder is redesigned using 0.18 μm technology for a comparison
Simulation was conducted with 5,000 random test patterns

- ❑ Achieves 19.1% power-and-delay product (PDP) reduction compared with conventional work
  - 23.1% power reduction with only 5.2% increased delay

** Y.-S. Wang et al., *IEEE ISCAS*, May 2011

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